

ABSTRACT

A semiconductor integrated circuit device with third gates comprising second conduction type source/drain diffusion layer regions 205 formed in first conduction type well 201, floating gates 203b formed on semiconductor substrate 200 through an insulator film 202, control gates 211a formed on floating gates 203b through nitrogen-introduced silicon oxide film 210a and third gates 207a different from the floating gates and the control gates, formed through the semiconductor substrates, the floating gates, the control gates and the insulator film, where the third gates are formed as filled in gaps between the floating gates existing in a vertical direction to word lines and channels and the height of third gates 207a thus formed is made lower than that of floating gates 203b, has improved reduction of memory cell size and operating speed and improved reliability after programming/erasing cycles.

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